Remarks

This application includes many claims and supporting technical description. Applicant is thus aware of and appreciates the unusual amount of time and analysis required by the Examiner to adequately review the application and prepare the Office Action.

Claims 1, 3-5, 10-11, 13-28, 30-31, 33-40 and 47 remain. Claims 2, 6-9, 12, 29, 32 and 41-46 have been canceled. Applicant acknowledges the allowance of claims 33-39.

In response to the Examiner's claim objection in paragraphs 6-7 of the Office Action, the phrase "word line" has been changed to "conductive word line" in claim 11.

The Saito 102(b) reference (U.S. 6,522,673 B2)

Claims 1-17, 20-32 and 40-47 have been rejected under Section 102(b) as being anticipated by U.S. 6,522,673 B2 (Saito et al.). Saito relates to a conventional MRAM that has the memory cells arrayed in a *single layer* on the substrate.

In Saito, all of the memory cells 20 (Fig. 1) lie in the same plane (often referred to as the "X-Y" plane in MRAM terminology). There are no "stacked" memory cells, i.e., no memory cells are on top of other cells along the Z direction perpendicular to the substrate, and thus no memory cell "column". Saito uses the unfortunate term "stacked", but this refers to the stacking (in the Z direction) of the individual layers in the individual memory cells, as described in column 8, lines 26-30. The Office Action states in lines 5-7 of paragraph 9 that Saito shows a "memory column (Figure 2) comprising a plurality of magnetic memory cells (20, 30) electrically coupled and stacked on top of each other". However, elements 30 are diodes, not memory cells, that are meant to represent the electrical equivalent of regions 12, 13, 14 in Fig. 1. This is explained in column 7, lines 34-43 and column 7, line 66 to column 8, line 3. Saito uses the unfortunate phrase "column direction" throughout the specification and claims, but this phrase clearly means either the X or Y direction, not the Z direction, as Saito explains throughout, e.g., "elements arrayed in a row direction and a column direction crossing the row direction" (column 2, lines 57-61).

More importantly, Saito teaches that it is *limited to a single layer of memory cells* in the X-Y plane and that it would be inoperative if multiple memory cells were stacked in the Z

direction. This is because the bit line 22 (Fig. 1) is in direct contact with the memory cells 20 and is used to write to the cells 20 (column 7, lines 7-15). If a second layer of memory cells was located below the memory cells 20 to thereby form "stacks" of memory cells, the memory cells in this additional layer would either be incapable of being written or would be undesirably written at the same time as the memory cells in the layer above were written. In either case, the result is an inoperative MRAM. Applicant points this out to also make it clear that, for this reason, Saito alone can not be a Section 103 reference because on its face Saito teaches away from Applicant's invention. Thus Saito alone would fail to state a *prima facie* case of obviousness against any of Applicant's remaining claims.

Amended independent claim 1

The Examiner's citation of Saito against Applicant's original claim 1 is understandable because the original claim 1 arguably did not clearly describe the direction of the stacking feature of Applicant's invention. Claim 1 has now been amended to move the stacking feature from the preamble into the elements of the claim. The "substrate" has been added to the claim elements and the "first memory cell column" now extends "perpendicularly from the substrate" and contains "stacked" memory cells. Similarly, the "first bit line column" now extends "perpendicularly from the substrate" "adjacent to the first memory cell column" and contains "stacked" conductive bit lines. This structure is shown in Figs. 1 and 2. In Fig. 1 the transistors 108 are on the substrate and memory cell columns 104 and bit line columns 110 extend in the Z direction perpendicularly from the substrate. Four layers of memory cells and adjacent bit lines are shown stacked in the Z direction in Fig. 1. Fig. 2 is a top view and shows the X-Y plane parallel to the substrate and shows the individual memory cells 220 in the top layer arrayed in X and Y rows (one of these X or Y rows would be referred to by Saito as a "column").

Since Saito does not show any of the claimed features in the above-quoted portions of Applicant's amended independent claim 1, and since each and every feature must be shown in an anticipating reference, Applicant's claim 1 is believed allowable and the rejection of claim 1 as being anticipated by Saito should be withdrawn.

Dependent claims 3-5, 10-11 and 13-19 now depend from allowable claim 1, and thus they too are believed to be allowable. (Applicant acknowledges that claims 18-19 were indicated to be allowable if amended to be in independent form).

Amended independent claim 20

Original claim 20 was rejected for substantially the same reason as original claim 1. Claim 2`0 has been amended in a manner similar to claim 1 and requires a "substrate", a "stack of magnetic memory cells extending perpendicularly from the substrate", and a "stack of bit lines extending perpendicularly from the substrate adjacent to the stack of memory cells".

In addition, claim 20 requires that each bit line is "configured to set a magnetic polarization within its adjacent associated magnetic memory cell" during *both* a memory write operation *and* a memory read operation. In Saito, the word lines 18, 19 (Fig. 1) (which would correspond to the bit lines in Applicant's invention) are used to change the magnetization of a memory cell *only* during a memory write, with no magnetization change during a memory read. In Saito, a memory read occurs in the conventional manner, with the use of bit line 22 (which would correspond to the word line in Applicant's invention), to detect the resistance across the memory cell. This is explained in Saito at column 9, lines 16-36.

Since Saito does not show any of the claimed features in the above-quoted portions of Applicant's amended independent claim 20, Applicant's claim 20 is believed allowable and the rejection of claim 20 as being anticipated by Saito should be withdrawn.

Dependent claim 21 now depends from allowable claim 20, and it too is believed to be allowable.

Amended independent claim 22

Original independent claim 22 has been rejected on the basis that Saito teaches the claimed method of writing to a memory cell. However, in Saito writing occurs by write currents through word lines 18, 19 simultaneous with write current through bit line 22 (Fig. 3A) to generate two magnetic fields that act as a composite magnetic field. In contrast, In Applicant's method of amended claim 22, a switch is turned on to "direct current from the word line *through* the memory cell" and a magnetic field is generating around a bit line "while current from the word line is passing through the memory cell". The current *through* the memory cell reduces the switching field, as explained in paragraphs [0033] and [0034] of the specification, which allows the write field from the bit line to align the magnetic polarization of the memory cell. This results in an alignment of the "magnetic polarization within the magnetic memory cell according to the direction of the magnetic field".

Since Saito does not show any of the claimed features in the above-quoted portions of Applicant's amended independent claim 22, in particular the feature of directing current *through* the memory cell during writing, Applicant's claim 22 is believed allowable and the rejection of claim 22 as being anticipated by Saito should be withdrawn.

Dependent claims 23-26 depend from allowable claim 22, and thus they too are believed to be allowable. Support for claims 24-26 is at paragraphs [0034] to [0036] of the specification.

Amended independent claim 27

Original independent claim 27 has been rejected on the basis that Saito teaches the claimed method of reading the magnetic state of a memory cell. However, in Saito, reading occurs by turning on appropriate transistors 201, 203 (Fig. 6) to allow current from bit line 22 to flow through memory cell 20 and diode 30 to word line 18. The electrical resistance across the memory cell can then be determined. (Column 9, lines 26-36). In contrast, in Applicant's method of amended claim 27, reading occurs by a two-step process of *first* "generating a magnetic field in a first direction around the bit line to thereby align a magnetic polarization within the memory cell according to said first direction of the magnetic field" and "measuring a resistance of the memory cell", and *then* "generating a magnetic field in a *second* direction opposite said first direction around the bit line to thereby *reverse the magnetic polarization* within the magnetic memory cell" and "measuring the resistance of the magnetic memory cell *with said reversed magnetic polarization*". This is explained in the specification at paragraphs [0039] to [0041] and [0061] and in steps 930-970 of Fig. 9.

Since Saito does not show the second portion of the claimed method 27, i.e., *reversing the magnetic polarization* and then *again measuring the resistance*, Applicant's claim 27 is believed allowable and the rejection of claim 27 as being anticipated by Saito should be withdrawn.

Dependent claims 28 and 30 depend from allowable claim 27, and thus they too are believed to be allowable.

Amended independent claim 31

Original independent claim 31 has been rejected on the basis that Saito teaches the claimed method of reading the magnetic state of a memory cell. The method of claim 31 is

similar to the method of claim 27 and is distinguishable over Saito for substantially the same reasons. In Applicant's method of claim 31, reading occurs by *first* "measuring the resistance of the magnetic memory cell", and *then* "generating a magnetic field around the bit line to thereby *reverse a magnetically pre-existing polarization* within the magnetic memory cell according to the direction of the magnetic field" and *again* "measuring the resistance of the magnetic memory cell". The method of claim 31 thus requires only a single application of magnetic field to the bit line to cause a magnetic polarization reversal, but two separate resistance measurements, one before the magnetic polarization reversal and one after, as explained in the specification in paragraph [0044].

Since Saito does not show a read process that includes a magnetic polarization reversal, and two separate resistance measurements, one before the magnetic polarization reversal and one after, as claimed in claim 31, Applicant's claim 31 is believed allowable and the rejection of claim 31 as being anticipated by Saito should be withdrawn.

Amended independent claim 40

Original claim 40 was rejected for substantially the same reason as original claim 1. Claim 40 has been amended to include many of the features of the now-canceled dependent claims 41-46. Claim 40 claims the structure described and shown in Figs 1 and 2 in terms of memory layers, with the "second memory layer on the first memory layer". For ease of understanding, the "first memory layer" can be considered the lowermost horizontal (X-Y plane) layer in Fig. 1 that comprises adjacent rows of memory cells and adjacent parallel bit lines (a "first row" of memory cells and "first" and "second" bit lines). The "second memory layer" is above this first memory layer and also comprises its own adjacent rows of memory cells and adjacent parallel bit lines (a "second row" of memory cells and "third" and "fourth" bit lines). Each of the memory cells in the second row is "stacked on and aligned with a corresponding memory cell in the underlying first row to form a memory cell column on the substrate". The third bit line is "stacked on and aligned with the underlying first bit line to form a first bit line column on the substrate", and the fourth bit line is "stacked on and aligned with the underlying second bit line to form a first bit line column on the substrate".

Since Saito does not show any of the claimed features in the above-quoted portions of Applicant's amended independent claim 40, Applicant's claim 40 is believed allowable and the

rejection of claim 40 as being anticipated by Saito should be withdrawn.

Amended independent claim 47

  Original claim 47 was rejected as being anticipated by Saito for the reason that Saito discloses a method of manufacturing a co-planar MRAM. Amended claim 47 claims the process as described in paragraph [0059] and shown in Fig. 7 of the specification. The process comprises "sequentially depositing a series of layers on a dielectric surface", and "thereafter patterning the deposited layers to *simultaneously* form a plurality of parallel rows of memory cells and a plurality of conductive bit lines parallel to the memory cell rows". Saito does not teach that the word lines 18, 19 and memory cells 20 (Fig. 1 of Saito) can be formed of the same stack of materials or "series of layers". More importantly, in Saito the memory cells 20 are in a *different layer above* the layer containing word lines 18, 19 so they can *not be simultaneously formed* in a single patterning step.

  Since Saito does not show any of the claimed features in the above-quoted portions of Applicant's amended independent claim 47, Applicant's claim 47 is believed allowable and the rejection of claim 1 as being anticipated by Saito should be withdrawn.

  The length and detail of this application and the relatively large number of claims has necessitated this rather lengthy amendment. Applicant is thus aware of and appreciates the unusual amount of time and analysis required by the Examiner to adequately review this amendment. For this reason, the Examiner is encouraged to call Applicant's undersigned attorney if a telephone discussion can expedite the prosecution of this application.

        Respectfully submitted,

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